REMARKS

The original dependent claims have been amended for clarity. Several paragraphs of the specification have also been editorially revised. Marked-up versions of the amended paragraphs and claims are attached to this Amendment.

Although not explicitly mentioned in the prior Amendment, it is apparent that independent Claims 6, 7, 12, 16, 20, 37, and 38 were amended analogously to Claim 1. So the noted distinction from Horiguchi's Fig. 37 also applies to those claims.

Claims 43-59 have been added to provide more comprehensive protection for several aspects of the invention, Claims 51-58 being independent. Claims 51-58 recite, inter alia, a first logic gate which is supplied with (or connected to receive) the first potential difference as a sole operation power source from a line pair, and a second logic gate which is supplied with (or connected to receive) the second potential difference as a sole operation power source from another line pair. Regarding Horiguchi's Fig. 37, note that circuit L41 is supplied with either of two potential differences defining

two operation power sources from line pair V_{CL}-V_{SL}, depending on the operation mode. By contrast, each of the first and second logic gates of the claimed invention receives but one potential difference as a sole operation power source from the corresponding line pair. Claims 51-58 thus also distinguish from Horiguchi's Fig. 37.

A Notice of Allowance is respectfully solicited.

A check in the amount of $510.00 is attached to cover the required additional claim fees.

The Commissioner is hereby authorized to charge to Deposit Account No. 50-1165 any fees under 37 C.F.R. §§ 1.16 and 1.17 that may be required by this paper and to credit any overpayment to that Account. If any extension of time is required in connection with the filing of this paper and has not been requested separately, such extension is hereby requested.

Respectfully submitted,

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August 30, 2002

Marked-up Copy of the Claims (Appln. No. 09/855,660):

2. (Amended) A semiconductor integrated circuit according to claim 1, wherein said first logic gate includes an MIS transistor to which a substrate bias is applied in a reverse direction by [said] a substrate potential, and said second logic gate includes an MIS transistor to which a substrate bias is applied in a forward direction by said substrate potential.

3. (Amended) A semiconductor integrated circuit according to claim 1, wherein said first logic gate includes a p-channel type MIS transistor and an n-channel type MIS transistor to which [a] substrate [bias is] biases are applied in a reverse direction by [said] respective substrate potentials, and said second logic gate includes a p-channel type MIS transistor and an n-channel type MIS transistor to which [a] substrate [bias is] biases are applied in a forward direction by [said] the respective substrate potentials.

4. (Amended) A semiconductor integrated circuit according to claim 1, wherein said first logic gate

includes a p-channel type MIS transistor to which a substrate bias is applied in a reverse direction by [said] a substrate potential, and said second logic gate includes a p-channel type MIS transistor to which a substrate bias is applied in a forward direction by said substrate potential.

5. (Amended) A semiconductor integrated circuit according to claim 1, wherein said first logic gate includes a p-channel type MIS transistor and an n-channel type MIS transistor to which [a] substrate [bias is] biases are applied in a reverse direction by [said] respective substrate potentials.

8. (Twice Amended) A semiconductor integrated circuit according to claim 6, wherein said first logic gate includes an MIS transistor to which a substrate bias is applied in a reverse direction by a potential in [said] the well region thereof, and said second logic gate includes an MIS transistor to which a substrate bias is applied in a forward direction by a potential in [said] the well region thereof.

9. (Twice Amended) A semiconductor integrated circuit according to claim 6, wherein said first logic gate includes a p-channel type MIS transistor and an n-channel type MIS transistor to which [a] substrate [bias is] biases are applied in a reverse direction by [the] respective potentials of [said] the well regions thereof, and said second logic gate includes a p-channel type MIS transistor and an n-channel type MIS transistor to which [a] substrate [bias is] biases are applied in a forward direction by [a] respective potentials of [said] the well regions thereof.

10. (Twice Amended) A semiconductor integrated circuit according to claim 6, wherein said first logic gate includes a p-channel type MIS transistor to which a substrate bias is applied in a reverse direction by a potential of [said] the well region thereof, and said second logic gate includes a p-channel type MIS transistor to which a substrate bias is applied in a forward direction by a potential in [said] the well region thereof.

11. (Twice Amended) A semiconductor integrated circuit according to claim 6, wherein said first logic gate includes a p-channel type MIS transistor and an n-channel

type MIS transistor to which [a] substrate [bias is] biases are applied in a reverse direction by [a] respective potentials in [said] the well regions thereof.

13. (Amended) A semiconductor integrated circuit according to claim 12, wherein said first potential pair includes a first high potential and a first low potential, said second potential pair includes a second high potential higher than said first high potential and a second low potential lower than said first low potential, and said substrate potential is one of a high potential side substrate potential between said first and second high potentials and [is] a low potential side substrate potential between said first and second low potentials.

17. (Amended) A semiconductor integrated circuit according to claim 16, wherein

said first potential line pair includes a first high potential line and a first low potential line,

said second potential line pair includes a second high potential line having a potential higher than that of said first high potential line and a second low potential line having a potential lower than said first low potential

line, and

said substrate potential line is one of a high potential side substrate potential line having a potential between the potential of said first high potential line and the potential of said second high potential line, and [is] a low potential side substrate potential line having a potential between the potential of said first low potential line and the potential of said second low potential line.

19. (Amended) A semiconductor integrated circuit according to claim 16, wherein said first potential line pair includes a first high potential line and a first low potential line,

said second potential line pair [is] includes said first low potential line and a second high potential line having a potential higher than that of the first high potential line [and is said first low potential line], and

said substrate potential line is one of a high potential side substrate potential line having a potential between the potential of said first high potential line and the potential of the second high potential line, and [is] a low potential side substrate potential line having a potential higher than the potential of said first low

potential line.

21. (Amended) A semiconductor integrated circuit according to claim 20, wherein said first logic gate includes an MIS transistor to which a substrate bias is applied in a reverse direction by [said] a substrate potential, and

said second logic gate includes an MIS transistor to which a substrate bias is applied in a forward direction by said substrate potential.

22. (Amended) A semiconductor integrated circuit according to claim 20, wherein said first logic gate includes a p-channel type MIS transistor and an n-channel type MIS transistor to which [a] substrate [bias is] biases are applied in a reverse direction by [said] respective substrate potentials, and

said second logic gate includes a p-channel type MIS transistor and an n-channel type MIS transistor to which [a] substrate [bias is] biases are applied in a forward direction by [said] the respective substrate potentials.

23. (Amended) A semiconductor integrated circuit

according to claim 20, wherein said first logic gate includes a p-channel type MIS transistor to which substrate bias is applied in a reverse direction by [said] a substrate potential, and

said second logic gate includes a p-channel type MIS transistor to which a substrate bias is applied in a forward direction by said substrate potential.

24. (Amended) A semiconductor integrated circuit according to claim 20, wherein said first logic gate includes a p-channel type MIS transistor and an n-channel type MIS transistor to which [a] substrate [bias is] biases are applied in a reverse direction by [said] respective substrate potentials.

37. (Twice Amended) A design data recording medium on which design data for forming an integrated circuit on a semiconductor chip is recorded so as to be readable by a computer, the design data comprising:

first mask pattern data for determining a figure pattern for forming a well region on which a plurality of logic gates is formed; [first logic gate to which an operation power source is supplied, in an active operation

mode, from a first pair of potential lines having a relatively small potential difference and a substrate potential is supplied from a substrate potential line on said semiconductor chip; and]

second mask pattern data for determining a figure pattern for forming a first line pair, a second line pair and a third line pair on said well region; [second logic gate to which an operation power source is supplied, in said active operation mode, from a second pair of potential lines having a relatively large potential difference and a substrate potential is supplied from a substrate potential line].

third mask pattern data for determining a figure pattern for forming a plurality of connectors,

wherein a first group of said connectors connects said first line pair and portions of said well region,

wherein a second group of said connectors connects said second line pair and a first group of said logic gates for supplying a first potential difference to said first group of logic gates in an active operation mode, and

wherein a third group of said connectors connects said third line pair and a second group of said logic gates for supplying a second potential difference which is larger

than said first potential difference to said second group of logic gates in said active operation mode.

39. (Amended) A semiconductor integrated circuit according to claim 7, wherein said first logic gate includes an MIS transistor to which a substrate bias is applied in a reverse direction by a potential in [said] the well region thereof, and said second logic gate includes an MIS transistor to which a substrate bias is applied in a forward direction by a potential in [said] the well region thereof.

40. (Amended) A semiconductor integrated circuit according to claim 7, wherein said first logic gate includes a p-channel type MIS transistor and an n-channel type MIS transistor to which [a] substrate [bias is] biases are applied in a reverse direction by [the] respective potentials of [said] the well regions thereof, and said second logic gate includes a p-channel type MIS transistor and an n-channel type MIS transistor to which [a] substrate [bias is] biases are applied in a forward direction by [a] respective potentials of [said] the well regions th reof.

41. (Amended) A semiconductor integrated circuit according to claim 7, wherein said first logic gate includes a p-channel type MIS transistor to which a substrate bias is applied in a reverse direction by a potential of [said] the well region thereof, and said second logic gate includes a p-channel type MIS transistor to which a substrate bias is applied in a forward direction by a potential in [said] the well region thereof.

42. (Amended) A semiconductor integrated circuit according to claim 7, wherein said first logic gate includes a p-channel type MIS transistor and an n-channel type MIS transistor to which [a] substrate [bias is] biases are applied in a reverse direction by [a] respective potentials in [said] the well regions thereof.

MARKED-UP COPY OF THE PARAGRAPHS

IN THE SPECIFICATION:

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Please substitute the following paragraph for the paragraph beginning at line 5:

The viewpoint of sharing the substrate potential may be also grasped from the viewpoint of sharing the well region in the MIS transistor. A semiconductor integrated circuit has: a first logic gate (1) using, as an operation power source, a first pair of potentials (VDDL and VSSL, VDDL and VSS) having a relatively small potential difference; and a second logic gate (2) using, as an operation power source, a second pair of potentials (VDDH and VSSH, VDDH and VSS) having a relatively large potential difference. Each of the first and second logic gates has an MIS transistor, and a well region (NWELL, PWELL) in which an MIS transistor in which the first logic gate is formed and a well region (NWELL, PWELL) of the MIS transistor in which the second logic gate is formed are made common every conduction type. According to the potential applied to the well region in the MIS transistor, the bias state of the MIS transistor is determined. The action at this time is the same as the above 1.

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Please substitute the following paragraph for the paragraph beginning at line 12:

Specific modes of the pair of the first and second potentials and the substrate potential are as follows. As a first mode, as shown in Fig. 1, the first potential pair includes a first high potential (VDDL) and a first low potential (VSSL), the second potential pair includes a second high potential (VDDH) higher than the first high potential and a second low potential (VSSH) lower than the first low potential, and the substrate potentials include a high potential side substrate potential (VBP) between the first and second high potentials and a low potential side substrate potential (VBN) between the first and second low potentials. In the mode, as described above, the reverse substrate bias state is achieved in both of the p-channel type MIS transistor and the n-channel type MIS transistor included in the first logic gate, and the forward substrate bias state is achieved in both of the p-channel type MIS transistor and the n-channel type MIS transistor included in the second logic gate.

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Please substitute the following paragraph for the paragraph beginning at line 19:

Figs. 19A and 19B schematically show power lines in a cell. Fig. 19A shows an example of a conventional cell layout having a pair of a power line interconnection and a ground line in a cell. Shown in Fig. 19A are a metal line 40 for transmitting the substrate potential VBP of a pMOS transistor, a metal line 41 for transmitting the power source potential VDD, a metal line 42 for transmitting the power source potential VSS, and a metal line 43 for transmitting the substrate potential VBN of an nMOS transistor. Fig. 19B shows an example of a layout of a cell such as a high-speed cell or low-power cell according to the invention. Shown in Fig. 19B are a metal line 44 for transmitting the substrate potential VBP of a pMOS transistor, a metal line 45 for transmitting a power source potential VDDH, a metal line 46 for transmitting the power source potential VDDL, a metal line 47 for transmitting the power source potential VSSL, a metal line 48 for transmitting the power source potential VSSH, and a metal line 49 for transmitting the substrate potential VBN of the nMOS transistor. In the case of a high-speed cell, the source of a MOS transistor is connected to the metal [liens] lines 45 and 48. In the case of a low-power cell, the source of a

MOS transistor is connected to the metal lines 46 and 47. By using a layout in which a plurality of power lines are arranged in a single cell as described above, the layout in which high-speed cells and low-power cells mixedly exist as shown in Fig. 17 is simplified. With respect to the width of the power line 41 in the conventional example of Fig. 19A and that of the power lines 45 and 46 in the layout according to the invention of Fig. 19B, since the invention provides the function of decreasing the power consumption of a circuit as described above, it is unnecessary to make the total of the widths of the power lines 45 and 46 wider than the width of the power line 41. Therefore, the cell size according to the layout of the invention does not become larger than that according to the conventional layout.